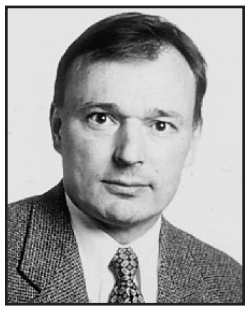
Session 23 Overview

Broadband RF and Radar

Chair: *Tom Schiltz, Linear Technology, Colorado Springs, CO*



Associate Chair: *Kari Halonen, Technical University of Helsinki, Espoo, Finland*

RF and microwave integrated circuit development is rapidly expanding into the millimeter-wave frequency range. Once the domain of exotic III-V semiconductor technologies, standard CMOS and BiCMOS are now well-suited for these applications. Significant factors driving RFIC development at these high frequencies are the availability of wideband unlicensed spectrum at 60GHz and the impressive speed capability of modern CMOS devices. New consumer applications include automotive radar at 79GHz and ultra-wideband (UWB) communication in the 3-to-10GHz band. These new consumer applications all require low-cost solutions, and modern CMOS and BiCMOS technologies are prepared to serve these new markets.

The eight papers in this session highlight several significant advances in broadband RFIC development. Paper 23.1 from NXP Semiconductors describes a broadband, 2-to-8GHz UWB receiver front-end realized in 65nm CMOS. This front-end IC incorporates a transformer-feedback LNA and a passive down-converting mixer to deliver high dynamic range with only 51mW of power consumption. Paper 23.2 from U Padova and Infineon also addresses UWB applications with a 3-to-5GHz LNA that includes an integrated notch filter to mitigate WLAN blockers. The LNA is implemented in 0.13μm CMOS and delivers 19dB of gain with 44dB of attenuation at the notch frequency.

Papers 23.3 and 23.4 present impressive wideband, inductor-less LNAs, each with 17dB of gain and sub-3dB noise figures. In Paper 23.3 by IMEC, DC-to-6GHz bandwidth with 2.8dB NF is achieved using a shunt-shunt feedback topology. This wideband LNA occupies an area of only 50x35μm^2. In Paper 23.4 by Linköping U, a differential LNA with current re-use has 7GHz of bandwidth and 2.4dB NF at 3GHz. Both of these LNA designs show significantly wider bandwidth than traditional source-degenerated designs, and occupy considerably less chip area since inductors are not required.

Following the break, the presentations include two papers that address radar and phased-array applications. Paper 23.5 from USC describes a 4-channel beam-forming receiver front-end for UWB applications in 0.13μm CMOS. The novel aspect of this beam-forming receiver is a path-sharing technique that reduces the die size. Paper 23.7 from Infineon and TU Vienna presents a 79GHz spread-spectrum transmitter for automotive radar applications implemented in BiCMOS. The RF output is BPSK-modulated at 1.235Gb/s and the output power is -1dBm.

Essential building blocks for millimeter-wave frequency synthesis are presented in Papers 23.6 and 23.8. Paper 23.6 from UCLA discusses frequency synthesis using the heterodyne phase locking technique. A series connection of mixers is used to generate various divide ratios with a lock range of 64 to 70GHz. The session concludes with Paper 23.8 by National Taiwan U, which presents a 75GHz PLL in 90nm CMOS. This PLL includes an integrated 75GHz VCO based on integrated transmission line resonators, with total power consumption of 88mW from a 1.45V supply.

23.1 A Broadband Receive Chain in 65nm CMOS **8:30 AM**

S. Lee, NXP Semiconductors, Eindhoven, The Netherlands

A fully integrated 65nm CMOS broadband RX front-end using a double-loop transformer-feedback LNA is presented. The frequency band from 2 to 8GHz is covered while the NF remains between 4.5 and 5.5dB and IIP3 is –7dBm. The active die area is 0.09mm^2 and the circuit consumes 51mW from a 1.2V supply.

23.2 A 0.13µm CMOS LNA with Integrated Balun and Notch Filter for 3-to-5GHz UWB Receivers **9:00 AM**

A. Vallese, University of Padova, Padova, Italy

A 0.13µm CMOS LNA for 3-to-5GHz UWB receivers embedding an integrated balun is reported. The LNA includes an integrated notch filter to mitigate the interference of WLAN blockers both in the UNII and ISM bands. Measured performance includes: voltage gain of 19.4dB, S_{11}<-10dB over the entire band, P_{1dB}>-9.4dBm, and maximum notch filter attenuation of 44dB. The LNA and the notch filter consume 24mW and 7.5mW, respectively.

23.3 An ESD-Protected DC-to-6GHz 9.7mW LNA in 90nm Digital CMOS **9:30 AM**

J. Borremans, IMEC, Leuven, Belgium

A 50×35µm^2 DC-to-6GHz LNA is designed in a digital 90nm CMOS process. It draws 8.1mA from a 1.2V supply and achieves a minimum NF of 2.8dB and 17dB of gain. In the 6GHz bandwidth, S_{11} is below -10dB and the IIP3 varies between -16 and -7dBm. ESD protection of 3.2kV HBM is implemented, as well as an optional second stage with gain selection adding up to 4dB of gain.

23.4 A 1.4V 25mW Inductorless Wideband LNA in 0.13µm CMOS **9:45 AM**

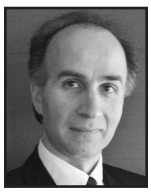
R. Ramzan, Linköping University, Linköping, Sweden

A 1.4V wideband inductorless LNA, implemented in a 0.13µm CMOS process, consumes 25mW and occupies 0.019mm^2. Measurement results show 17dB voltage gain, 7GHz BW, 2.4dB NF at 3GHz, -4.1dBm IIP3, and -20dBm P_{1dB}. A common-drain feedback circuit provides wideband 50Ω input matching and partial noise cancellation. A current reuse technique improves both gain and power.

23.5 A Monolithic 4-Channel UWB Beam-Former in 0.13µm CMOS Using a Path-Sharing True-Time-Delay Architecture

T-S. Chu, University of Southern California, Los Angeles, CA **10:15 AM**

A fully integrated 4-channel UWB beam-former in 0.13µm CMOS uses a path-sharing true-time-delay architecture with 15ps resolution. The 3.1×3.2mm^2 chip produces 11 different scanning angles within ±60° with 10° spatial resolution for 25mm antenna spacing. The front-end achieves an NF of 2.9 to 4.8dB across 18GHz of BW with less than 5ps of group delay variation.



23.6 Heterodyne Phase Locking: A Technique for High-Frequency Division **10:45 AM**

B. Razavi, University of California, Los Angeles, CA

The use of multiple downconversion mixers in a PLL can provide frequency division with arbitrary integer or fractional divide ratios. A heterodyne PLL, realized in a 0.13µm CMOS process, achieves a lock range of 64GHz to 70GHz with no external tuning. The circuit consumes 6mW from a 1.2V supply.

23.7 A 79GHz SiGe-Bipolar Spread-Spectrum TX for Automotive Radar **11:15 AM**

S. Trotta, Infineon, Munich, Germany

A 79GHz spread-spectrum TX, implemented in a SiGe Bipolar process, consists of a VCO, a prescaler, a PRBS generator, and a biphase modulator. The sequence length of the PRBS is 1023 bits at a bit rate of 1.235Gb/s. The chip provides an output power of -1dBm and draws 750mA from a 5.5V supply.

23.8 A 75GHz PLL in 90nm CMOS **11:45 AM**

J. Lee, National Taiwan University, Taipei, Taiwan

The design and experimental verification of a 75GHz PLL implemented in a 90nm CMOS process are presented. The circuit incorporates a three-quarter wavelength oscillator and a PFD based on SSB mixers and achieves an operation range of 320MHz and reference sidebands of less than -72dBc while consuming 88mW from a 1.45V supply.